

# **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

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Application Number	<del>10882468</del> 10/822,468
Filing Date	2004-04-12
First Named Inventor	Mitchell Alsup
Art Unit	2183
Examiner Name	George D. Zalepa
Attorney Docket Number	5500-92000

1/9/07

W	6	Hinton, G., et al., "A 0.18-MUM CMOS IA-32 Processor with a 4-GHZ Integer Execution Unit," IEEE Journal of Solid-State Circuits, Vol. 36, No. 11, November 2001, pages. 1617-1627.	<input type="checkbox"/>
W	7	Palmer, et al., "Fido: A Cache That Learns to Fetch," Proceedings of the 17th International Conference on Very Large Data Bases, Barcelona, September 1991, pp. 255-264.	<input type="checkbox"/>
W	8	Chen et al., "Eviction Based Cache Placement for Storage Caches," USENIX 2003 Annual Technical Conference, (13 pages).	<input type="checkbox"/>
W	9	Merten, et al., "An Architectural Framework for Run-Time Optimization," June 2001, pp. 1-43.	<input type="checkbox"/>
W	10	Jourdan, et al., "Increasing the Instruction-Level Parallelism through Data-Flow Manipulation," Intel, 11 pages.	<input type="checkbox"/>
W	11	Bryan Black, et al., "Turboscalar: A High Frequency High IPC Microarchitecture," Dept. of Electrical and Computer Engineering, Carnegie Mellon Univ., June 2000.	<input type="checkbox"/>
W	12	Grant Braught, "Clas #21-Assemblers, Labels & Pseudo Instructions," Dickenson College, Fall Semester 2000, 6 pages.	<input type="checkbox"/>
W	13	U.S. Application Serial No. 10/676,437 filed 10/1/03, Alsup, et al.	<input type="checkbox"/>
W	14	U.S. Application Serial No. 10/615,506 filed 7/8/03, Alsup	<input type="checkbox"/>
W	15	U.S. Application Serial No. 10/755,742 filed 1/12/04, Smaus, et al.	<input type="checkbox"/>

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